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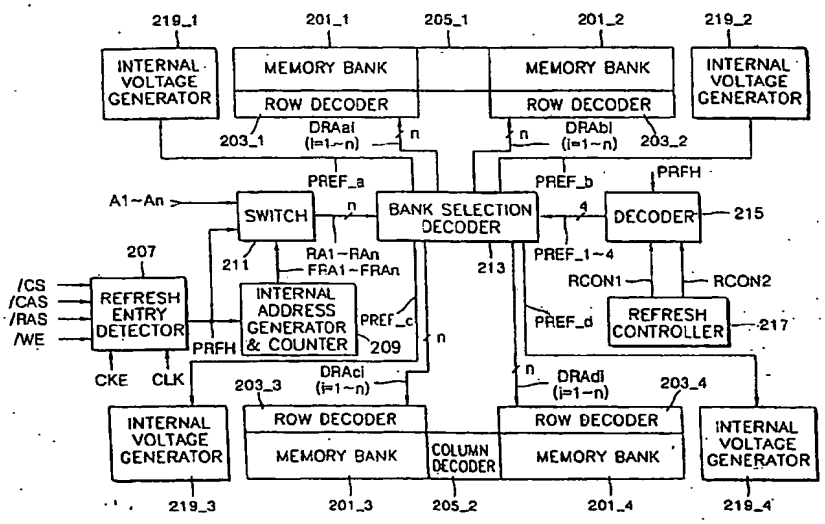
(54) System and method for performing partial array self-refresh operation in a semiconductor memory device.

(57) Systems and methods for performing a PASR (partial array self-refresh) operation wherein a refresh operation for recharging stored data is performed on a portion (e.g., ½ 1/4, 1/8, or 1/16) of one or more selected memory banks comprising a cell array in a semiconductor memory device. In one aspect, a PASR operation is performed by (1) controlling the generation of row addresses by a row address counter during a self-refresh operation and (2) controlling a self-refresh cycle generating circuit to adjust the self-refresh cycle output therefrom. The self-refresh cycle is adjusted in a manner that provides a reduction in the current dissipation during the PASR operation. In another aspect, a PASR operation is performed by controlling one or more row addresses corresponding to a partial cell array during a self-refresh operation, whereby a reduction in a self-refresh current dissipation is achieved by blocking the activation of a non-used block of a memory bank.

FIG. 2



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of the present invention to provide a semiconductor memory device, such as a dynamic random access memory (DRAM), having a plurality of memory banks, wherein the semiconductor memory device is capable of selectively performing a self-refresh operation with respect to individual memory banks and with respect to a portion of one or more selected memory banks.

[0012] The present invention provides various mechanisms for performing a PASR (partial array self-refresh) operation wherein a refresh operation for recharging stored data is performed on a portion of one or more selected memory banks comprising a cell array in a semiconductor memory device. More specifically, the present invention provides mechanisms for performing a PASR operation for, e.g., ½ 1/4, 1/8, or 1/16 of a selected memory bank.

[0013] In one aspect of the present invention, a PASR operation is performed by (1) controlling the generation of row addresses by a row address counter during a self-refresh operation and (2) controlling a self-refresh cycle generating circuit to adjust the self-refresh cycle output therefrom. The self-refresh cycle is adjusted in a manner that provides a reduction in the current dissipation during the PASR operation.

[0014] In another aspect of the present invention, a PASR operation is performed by controlling one or more row addresses corresponding to a partial cell array during a self-refresh operation, whereby a reduction in a self-refresh current dissipation is achieved by blocking the activation of a non-used block of a memory bank.

[0015] In yet another aspect of the present invention, a memory device comprises:

a plurality of memory banks each comprising a plurality of memory blocks; and
a self-refresh controlling circuit for selecting one of the memory banks and performing a self-refresh operation on one of the memory blocks of the selected memory bank.

[0016] In another aspect, a circuit for performing a PASR operation in a semiconductor memory device comprises:

a first pulse generator for generating a self-refresh cycle signal during a refresh operation of a semiconductor memory device, wherein the self-refresh cycle signal comprises a predetermined period T; and
a counter comprising a plurality of cycle counters for generating row address data in response to the self-refresh cycle signal, wherein the row address data is decoded to activate wordlines of a memory bank during the refresh operation of the semiconductor memory device,

wherein during a PASR operation, the counter is responsive to PASR control signal to disable operation of a cycle counter to mask an address bit output from the counter and wherein the first pulse generator is responsive to the PASR control signal to increase the predetermined period T of the self-refresh cycle signal.

[0017] In yet another aspect, a circuit for performing a PASR operation in a semiconductor memory device comprises:

a first pulse generator for generating a self-refresh cycle signal during a refresh operation of a semiconductor memory device;
a counter comprising a plurality of cycle counters for generating row address data in response to the self-refresh cycle signal, wherein the row address data is decoded to activate wordlines of a memory bank during the refresh operation of the semiconductor memory device;
a row address buffer for receiving the row address data output from the counter and outputting row addresses;
a row predecoder for decoding the row addresses output from the row address buffer to generate self-refresh address signals that are processed to activate wordlines of a memory bank during the refresh operation of the semiconductor memory device,

wherein during a PASR operation, the row address buffer is responsive to a PASR control signal to mask one or more address bits of the row address data to block activation of wordlines corresponding to a non-used portion of a memory bank.

[0018] In another aspect of the present invention, a circuit for performing a PASR operation in a semiconductor memory device comprises:

a first pulse generator for generating a self-refresh cycle signal during a refresh operation of a semiconductor memory device;
a counter comprising a plurality of cycle counters for generating row address data in response to the self-refresh cycle signal, wherein the row address data is decoded to activate wordlines of a memory bank during the refresh operation of the semiconductor memory device;
a row address buffer for receiving the row address data output from the counter and outputting row addresses;
a row predecoder for decoding the row addresses output from the row address buffer to generate self-refresh address signals that are processed to activate wordlines of a memory bank during the refresh operation of the semiconductor memory device,

wherein during a PASR operation, the row predecoder is responsive to a PASR control signal to mask one or more address bits of the row address data to block activation of wordlines corresponding to a non-used portion of a memory bank.

equally applicable to DRAMs having a plurality of memory banks other than four in number.

[0023] The respective memory_banks 201_i have a plurality of memory cells arranged in columns and rows. Row decoders 203_i designate row addresses in the corresponding memory banks. For example, the row decoder 203_1 selects a row address in the memory bank 201_1.

[0024] Column decoders 205_1 and 205_2 designate column addresses in the corresponding memory banks. For example, the column decoder 205_1 selects column addresses in the memory banks 201_1 and 201_2.

[0025] In response to entry into a self-refresh mode, a refresh entry detector 207 generates a refresh instruction signal PRFH. In other words, if the self-refresh mode is entered, the refresh instruction signal PRFH is activated to a logic "high" level. The structure and operation of the refresh entry detector 207 will later be described in detail with reference to FIG. 3.

[0026] An internal address generator and counter 209 generates a pulse for each predetermined period during a self-refresh operation and generates counting addresses FRA1 to FRAn sequentially increasing in response to the pulses. The combination of the counting addresses FRA1 to FRAn sequentially changes the designated row addresses. A switch 211, activated by the refresh instruction signal PRFH generated in the refresh entry detector 207, receives external addresses A1 to An during operation in a normal mode and receives the counting addresses FRA1 to FRAn during operation in the refresh mode, and, in turn, generates internal addresses RA1 to RAn. The operation of the switch 211 will later be described in detail with reference to FIG. 5.

[0027] Referring back to FIG. 2, in addition to the circuits included in the conventional DRAM, the DRAM of the present invention further includes a bank selection decoder 213, a decoder 215 and a refresh controller 217. The decoder 215 and the refresh controller 217 are preferably implemented by a refresh bank designating circuit of the present invention, described below. Also, the bank selection decoder 213, the decoder 215 and the refresh controller 217 can be implemented by a refresh controlling'circuit of the present invention, described below

[0028] The decoder 215 generates first through fourth refresh bank designating signals PREF_i (Here, i is an integer from 1 to 4). Memory banks 201_1 to be refreshed are determined by the first through fourth refresh bank designating signals PREF_1 to PREF_4.

[0029] The refresh controller 217 generates refresh control signals RCON1 and RCON2 and supplies the same to the decoder 215. There may be more than the two refresh control signals RCON1 and RCON2. The refresh control signals RCON1 and RCON2 control selection of memory banks to be refreshed. The refresh controller 217 will be described in detail below with reference to FIGS. 6, 7 and 8.

[0030] The decoder 215 decodes the refresh control signals RCON1 and RCON2 in a self-refresh mode to generate the first through fourth refresh bank designating signals PREF_1 to PREF_4. The decoder 215 will later be described in detail with reference to FIG. 9.

[0031] The bank selection decoder 213 receives the first through fourth refresh bank designating signals PREF_1 to PREF_4 and the internal addresses RA1 to RAn in the self-refresh mode. The bank selection decoder 213 supplies refresh addresses DRAai (where i is an integer from 1 to 4) to the row decoders of the memory banks selected by the first through fourth refresh bank designating signals PREF_1 to PREF_4 and a combination thereof.

[0032] For example, in the case where the first memory bank 201_1 (FIG. 2) is selected by the first through fourth refresh bank designating signals PREF_1 to PREF_4 to then be refreshed, the data of the internal addresses RA1 to RAn is supplied as the refresh addresses DRAa1 to DRAa4 to the row decoder 203_1 which selects a row address of the memory cell of the memory bank 201_1. The bank selection decoder 213 will later be described in detail with reference to FIGS. 10 through 13.

[0033] The internal voltage generators 219_i (where i is an integer from 1 to 4) supply DC voltages to circuits associated with the respective memory banks 201_i, and may include one or more circuits selected from a back-bias voltage generator, an internal power-supply voltage generator and other internal voltage generating circuits. In the DRAM of the present invention, the internal voltage generators 113_i exist for each memory bank and are enabled to be driven only when a self-refresh operation is performed on the corresponding memory bank. Here, for the sake of convenience in explanation, with respect to a self-refresh mode, the case where the internal voltage generators 219_i are enabled for each memory bank is representatively described. However, it is evident to one skilled in the art that the present invention can be applied to all operation modes in addition to the self-refresh mode.

[0034] Typical examples of the internal voltage generators 219_i (i=1...4) will later be described in detail with reference to FIG. 14.

[0035] FIG. 3 is a detailed circuit diagram of the refresh entry detector 207 shown in FIG. 2, and FIG. 4 is a timing diagram of various signals shown in FIG. 3. Referring to FIGS. 3 and 4, the structure and operation of the refresh entry detector 207 will now be described.

[0036] The refresh entry detector 207 includes an entry detecting part 301, a latching part 303 and a termination detecting part 305. The entry detecting part 301 detects the entry into a self-refresh mode by means of an internal clock signal PCLK, a first internal clock enable signal PCKE1, a chip selection signal /CS, a column address strobe signal /RAS and a write enable signal /WE. In other words, if a semiconductor memory device enters into a self-refresh mode, the output signal N302 of the entry detecting part 301 makes a transition to a

the case where there is further provided an apparatus for performing cutting of the control fuses FUSE1 and FUSE2 by address information for designating the memory bank for storing data, the refresh operation in the DRAM of the present invention can be performed only with respect to the memory bank in which data is stored.

[0051] FIG. 8 is still another circuit diagram of the refresh controller 217 shown in FIG. 2, in which refresh control signals are generated by external addresses, like in FIG. 6. Referring to FIG. 8, the refresh controller 217 includes a transfer gate 801 and a latch 803. The transfer gate 801 receives external addresses A10 and A11 during a period in which a first internal clock enable signal PCKE1 and an internal clock signal PCLK are in a logic "high" level. The latch 803 latches the external addresses A10 and A11 transferred by the transfer gate 801 to generate the refresh control signals RCON I and RCON2. In other words, in the case where the external addresses A10 and A11 are at a logic "high" level, the refresh control signals RCON1 and RCON2 are latched to a logic "high" level. Also, in the case where the external addresses A10 and A11 are at a logic "low" level, the refresh control signals RCON1 and RCON2 are latched to a logic "low" level.

[0052] FIG. 9 is a detailed circuit diagram of the decoder 215 shown in FIG. 2. Referring to FIG. 9, the decoder 215 includes four NAND gates 909, 911, 913 and 915 enabled during operation in a refresh mode in which the refresh instruction signal PRFH is at a logic "high"level, and another group of four NAND gates 901, 903, 905 and 907 for decoding the refresh control signals RCON1 and RCON2.

[0053] In the refresh mode, if the refresh control signals RCON1 and RCON2 are both at a logic "low" level, the output signal N902 of the NAND gate 901 becomes "low". In response, the first refresh bank designating signal PREF_1 which is the output signal of the NAND gate 909, becomes "high".

[0054] In the refresh mode, if the refresh control signal RCON1 is at a logic "high" level, and RCON2 is at a logic "low" level, the output signal N904 of the NAND gate 903 becomes "low". In response, the second refresh bank designating signal PREF_2, which is the output signal of the NAND gate 911, becomes "high".

[0055] In the refresh mode, if the refresh control signals RCON1 is at a logic "low" level, and RCON2 is at a logic "high" level, the output signal N906 of the NAND gate 905 becomes "low". In response, the third refresh bank designating signal PREF_2, which is the output signal of the NAND gate 913, becomes "high".

[0056] In the refresh mode, if the refresh control signals RCON1 and RCON2 are both at a logic "high" level, the output signal N908 of the NAND gate 907 becomes "low". The fourth refresh bank designating signal PREF_4, which is the output signal of the NAND gate 915, becomes "high".

[0057] FIG. 10 is a circuit diagram of the bank selection decoder 213 shown in FIG. 2, in which a bank is selected by a refresh bank designating signal. Referring to FIG. 10, the bank selection decoder 213 includes four buffers 1001, 1003, 1005 and 1007 and four pre-decoders 1011, 1013, 1015 and 1017.

[0058] The buffers 1001, 1003, 1005 and 1007 buffer the first through fourth refresh bank designating signals PREF_1 through PREF_4 to generate first through fourth decoding signals PREF_j (j=a, b, c and d). Thus, the first through fourth decoding signals PREF_a through PREF_d represent the same information as that of the first through fourth refresh bank designating signals PREF_1 through PREF_4. Referring back to FIG. 2, the first through fourth decoding signals PREF_a through PREF_d are supplied to the internal voltage generators 219_1 through 219_4, respectively, to control the same.

[0059] Referring back to FIG. 10, the pre-decoders 1011, 1013, 1015 and 1017 are enabled in response to the first through fourth decoding signals PREF_a through PREF_d. Also, the enabled pre-decoders 1011, 1013, 1015 and 1017 receive internal addresses RA1 to RAn to generate refresh addresses DRAji (where j=a, b, c and d and i=1 to n.). The pre-decoders 1011, 1013, 1015 and 1017 will be described later in more detail with reference to FIGS. 11 and 12.

[0060] The operation of the bank selection decoder 213 shown in FIG. 10 will now be described for the case in which the first refresh bank designating signal PREF_1 is activated. If the first refresh bank designating signal PREF_1 is activated, the first decoding signal PREF_a is activated. As the first decoding signal PREF_a is activated, the first pre-decoder 1011 is enabled. Thus, the first refresh addresses DRAai (i=1 to n) have the same information as the internal addresses RA 1 to RAn. The first refresh addresses DRAai (i=1 to n) are transferred to the first row decoder 203_1 for decoding rows of the first memory bank 201_1 (FIG. 2) to then refresh memory cells of the first memory bank 201_1.

[0061] When the first refresh bank designating signal PREF_1 is activated in the bank selection decoder 213, the second through fourth refresh bank designating signals PREF_2 through PREF_4 are deactivated and the second through fourth pre-decoders 1013, 1015 and 1017 are disabled. Thus, the second through fourth refresh addresses DRAji, (j=b, c and d, and i=1 to n.) are maintained at a logic "low" level, which is a precharged state. Thus, the refresh operation is not performed on the memory cells of the second through fourth memory banks 201_2 through 201_4. In the case of implementing a DRAM capable of selectively performing a refresh operation for each bank using the bank selection decoder 213 shown in FIG. 10, only one memory bank is selected and then refresh addresses are supplied thereto.

[0062] Referring back to FIGS. 9 and 10, banks are selected based on the refresh control signals RCON1 and RCON2 as follows.

RA1 to RAn. Thus, the first and second memory banks 201_1, 201_2, 201_3 and 201_4 perform a refresh operation.

[0075] The first through fourth pre-decoders 1311, 1313, 1315 and 1317 shown in FIG. 13 can be implemented by the same configuration as the predecoders1011, 1013, 1015 and 1017 shown in FIG. 10, and a detailed explanation thereof will be omitted.

[0076] The bank selection decoder 213 shown in FIG. 13 can have a variable number of pre-decoders. Also, in the DRAM capable of selectively performing a refresh operation according to the present invention, it is possible to selectively refresh only those memory banks having memory cells in which data is stored. Also, the number of refreshed memory banks can be varied by using the bank selection decoder shown in FIG. 13.

[0077] FIG. 14 is a circuit diagram of an internal voltage generator shown in FIG. 1, in which an internal power-supply voltage generator is illustrated as an example of the internal voltage generator. However, it is evident to one skilled in the art that the invention can also be applied to a back-bias voltage generator. Also, although a first internal voltage generator 219_1 is representatively illustrated, the present invention can be applied to second through fourth internal voltage generators 219_i (i=2 to 4).

[0078] First, in the case where a refresh operation is performed with respect to a first memory bank 201_1 (see FIG. 2), a first decoding signal PREF_a goes "high". Then, PMOS transistors 1401 and 1405 are turned off and an NMOS transistor 1407 is turned on. Thus, the internal power-supply voltage generator shown in FIG. 14 is enabled to generate an internal power supply voltage PIVG, as in the conventional art. Since the operational principle of generating the internal power supply voltage PIVG is well known to one skilled in the art, a detailed explanation thereof will be omitted.

[0079] In the case where a refresh operation is not performed with respect to the first memory bank 201_1, the first decoding signal PREF_a goes "low". Then, the PMOS transistors 1401 and 1405 are turned on and the NMOS transistor 1407 and a PMOS transistor 1403 are turned off. Thus, the internal power-supply voltage generator shown in FIG. 14 is disabled to stop operating. As described above, the internal power-supply voltage generator shown in FIG. 14 operates such that only the internal voltage generator corresponding to a memory bank on which the refresh operation is performed operates. Thus, the internal voltage generator corresponding to a memory bank on which the refresh operation is not performed stops operating, thereby greatly reducing power consumption.

[0080] In addition to the preferred embodiments described above for performing a full array self-refresh on one or more selected memory banks of a memory cell, other embodiments of the present invention provide mechanisms for performing a PASR (partial array self-refresh) operation for a portion (one or more blocks) of one or more selected memory banks. More specifically, the present invention provides mechanisms for performing a PASR operation for, e.g., ½, 1/4, 1/8, or 1/16 of a selected memory bank. In general, in one embodiment of the present invention, a PASR operation is performed by (1) controlling the generation of row addresses by a row address counter during a self-refresh operation and (2) controlling a self-refresh cycle generating circuit to adjust the self-refresh cycle output therefrom. As explained below, the self-refresh cycle is adjusted in a manner that provides a reduction in the current dissipation during the PASR operation. In another embodiment, a PASR operation is performed by controlling one or more row addresses corresponding to a partial cell array during a self-refresh, whereby a reduction in a self-refresh current dissipation is achieved by blocking the activation of a non-used block of a memory bank.

[0081] Figs. 15a and 15b illustrate exemplary array divisions of one memory bank "B" of a plurality of memory banks in a semiconductor memory device. As explained above, a memory cell array of a semiconductor device can be divided into several memory banks using bank address coding (e.g., addresses A12 and A13 can be used to generate 4 memory banks). Furthermore, in accordance with the present invention, as illustrated in Fig. 15a, a memory bank B is logically divided into two blocks (Block 1, Block 2), preferably of equal size, using address coding of one address (e.g., A11). During a partial array self-refresh operation, Block 1 is accessed in response to address A11 of logic level "low" or Block 2 is accessed in response to address A11 of logic level "high". In other words, during a partial array self-refresh operation, self-refresh is performed on only one-half(½) of the memory bank (e.g., self-refresh is performed on Block 1 and not on Block 2).

[0082] Further, in Fig. 15b, a memory bank B is logically divided into four blocks (Block 1, Block 2, Block 3 and Block 4), preferably of equal size, using address coding of two addresses (e.g., A 10, A11). During a partial self-refresh operation, one of Blocks 1-4 can be accessed by the corresponding address. For example, Block 1 is accessed in response to address A11 and A10 of logic level "low" and Block 2 is accessed in response to A11 of logic level low and A 10 of logic level "high". In other words, during a partial array self-refresh operation, self-refresh is performed on only one-quarter (1/4) of the memory bank (e.g., self-refresh is performed on Block 1 and not on Blocks 2-4). Likewise, a memory bank can be logically divided into 8 and 16 blocks respectively using 3 and 4 addresses (and so on), wherein a 1/8 or a 1/16 block of the memory bank is self-refreshed. A more detailed description of preferred embodiments for performing a PASR operation will now be described.

[0083] Fig. 16 is a schematic of a circuit for performing PASR operation according to an embodiment of the present invention. Fig. 16 illustrates an embodiment of the internal address generator and counter 209 shown

1604-4, so that the period of the PSELF signal that is generated is twice the period (2T) of the predetermined self-refresh cycle for the full array self-refresh operation. For each additional counter used, the period T of PSELF is doubled. For Instance, Fig. 20 is a diagram illustrating world line activation intervals for a full array self-refresh operation, a ½ PASR operation and a 1/4 PASR operation. Thus, for the 1/4 PASR operation, the use of two additional counters in the PSELF generator 1603 will cause the period of the PSELF signal to quadruple (4T) from the predetermined period T of the full array self-refresh operation.

[0093] Fig. 21 is a schematic of a circuit for performing PASR operation according to another embodiment of the present invention. The operation of the circuit of Fig. 21 is similar to the operation of the circuit of Fig. 16 as described above, except that counter10 1605-10 and counter11 1605-11 are selectively disabled/enabled by a control signal IN3 which is input to the PSELF generator for controlling the self-refresh interval. By selectively disabling both cycle counter 10 and cycle counter11 via control signal IN3, address bits CNT10 and CNT11 can respectively be masked and fixed to desired levels, so as to perform a 1/4 PASR operation.

[0094] Fig. 22 illustrates an embodiment of a self-refresh cycle generating circuit 1603 according to the present invention, in which a refresh cycle is selectively controlled by control signals IN2 and IN3 to double or quadruple the predetermined self-refresh cycle "T". The circuit comprises a plurality of cycle counters 1604, 1605, 1606 and 1607, a NOR gate 1608, a plurality of transfer gates 1609, 1610, 1611, and a plurality of inverter buffers 1612, 1613, 1614, all of which are operatively connected as shown. The control signal 1N2 is used to enable a ½ PASR operation and the control signal IN3 is used to enable a 1/4 PASR operation. Depending on the logic levels of the control signals IN2 and IN3, the path of the oscillator signal POSC will vary to obtain the desired PSELF signal output from the Q1 cycle counter 1604.

[0095] More specifically, assume that the output of cycle counter 1604 is the output that determines a current cycle. In one embodiment, in case of a full array self-refresh operation, the signals IN2 and IN3 are fixed to have a logic "low" level. The transfer gate 1609 is activated and the transfer gates 1610 and 1611 are not activated, which causes the signal POSC to pass through cycle counters 1605 and 1604 to generate a PSELF signal having period "T" (as shown in the timing diagram of Fig. 23a). In case of ½ PASR operation, the signals IN2 and IN3 are fixed to have a logic "high" level and a logic "low" level, respectively. As a result, transfer gates 1609 and 1611 are not activated and the POSC signal passes through cycle counters 1606, 1605 and 1604. The output of counter 1604 (PSELF) has a period that is twice the period of the PSELF for the full array self-refresh (as shown in the timing diagram of Fig. 23b). Further, in case of a 1/4 PASR operation, the signals IN2 and IN3 are fixed to have a logic "low" level and a logic "high" level, respectively, which results in transfer gate 1611 being activated and transfer gates 1609 and 1610 not being activated. The POSC signal therefor passes through all of the cycle counters 1606, 1607, 1605 and 1604. The output signal of counter 1604 will thus have a period that four times the predetermined period "T" for the full array self-refresh (as illustrated in the timing diagram of Fig. 23c).

[0096] Figs. 24(a) and 24(b)are schematic diagrams illustrating cycle counters according to another embodiment of the present invention. In particular, Figs 24(a) and 24(b) illustrate embodiments for cycle counters 1605-11 and 1605-10 that can be implemented in the counter 1605 of diagram 21 for providing, e.g., a 1/4 PASR operation, according to an embodiment of the present invention. The exemplary cycle counters shown in Figs 24(a) and 24(b) are similar to the cycle counter illustrated in Fig. 18(a), except for the inclusion of buffer inverter I6, and transfer gates t5 and t6, which are operatively connected as shown. In addition, the control signals IN2 and IN3 each comprise a two bit signal, IN2A, IN2B and IN3A, IN3B, respectively, for providing various outputs of counter bits CNT11 and CNT10, which in turn provide various outputs of the address bits 10 and 11 for selecting a block of memory of a selected memory bank. For instance, in one embodiment, one of Blocks 1-4 of selected memory bank are refreshed based on a 1/4 PASR operation in accordance with the following table:

IN3	IN2	Block
IN3B/IN3A	IN2B/IN2A	
L / L	L / L	1
H / L	L / L	2
L / L	H / L	3
H / L	H / L	4

[0097] In accordance with another embodiment of the present invention, a second control method for performing a PASR operation is one which controls not a corresponding row address counter, but rather a row address corresponding to a partial cell array of the row address, and blocks an activation of non-used blocks of a selected memory bank. For instance, referring again to Fig. 15a, cell data are amplified in connection with a self-refresh counter in Block1. In Block2, even though the self-refresh counter is enabled, an activation is blocked in a manner that controls not a self-refresh address counter but an address. Blocking the activation is performed by blocking a row address applied to a row address buffer or decoder.

[0098] Fig. 25 is a schematic diagram of the row address buffer 1606 illustrating a method of blocking an activation of a row address via the row address buffer.

memory bank during the refresh operation.

8. A method according to Claim 7, wherein the step of selecting a block of memory cells in the selected m mory bank comprises the steps of:

generating a self-refresh command signal;
masking one or more bits of row address data in response to the self-refresh command signal; and
selecting for the refresh operation, the block of memory cells addressed by the masked bits.

9. A method according to Claim 8, wherein the step of masking the bits comprises level-fixing the bits.

10. A method according to Claim 9, wherein the block of memory cells are selected based on the fixed value of the masked bits.

11. A method according to Claim 8, further comprising the steps of:

generating a self-refresh cycle signal for controlling the refresh operation; and
increasing the period of the self-refresh cycle signal based on the self-refresh command signal.

12. A method for controlling a self-refresh operation in a semiconductor memory device, comprising the steps of:

generating a control signal during a self-refresh operation;
masking at least one row address in response to the control signal;
performing a self-refresh operation for a portion of a memory bank in the semiconductor memory device using unmasked row addresses.

13. A method according to Claim 12, wherein the step of masking at least one row address comprises disabling operation of a cycle counter to level-fix an address bit.

14. A method according to Claim 13, further comprising the step of increasing a period of a self-refresh cycle signal in response to the control signal.

15. A method according to Claim 12, further comprising the step of selecting a portion of the memory bank using the masked address.

16. A method according to Claim 12, wherein the step of masking at least one row address comprises the step of blocking activation of a row address corresponding to a non-used portion of the memory bank.

17. A method according to Claim 16, wherein the step of blocking activation of a row address is performed in a row address buffer.

18. A method according to Claim 16, wherein the step of blocking activation of a row address is performed in a row address pre-decoder.

19. A circuit for performing a PASR (partial array self refresh) operation in a semiconductor memory device, the circuit comprising:

a first pulse generator for generating a self-refresh cycle signal during a refresh operation of a semiconductor memory device, wherein the self-refresh cycle signal comprises a predetermined period T; and
a counter comprising a plurality of cycle counters for generating row address data in response to the self-refresh cycle signal, wherein the row address data is decoded to activate wordlines of a memory bank during the refresh operation of the semiconductor memory device,

wherein during a PASR operation, the counter is responsive to PASR control signal to disable operation of a cycle counter to mask an address bit output from the counter and wherein the first pulse generator is responsive to the PASR control signal to increase the predetermined period T of the self-refresh cycle signal.

20. A circuit according to Claim 19, further comprising a command buffer for receiving an external self-refresh command signal and outputting the PASR control signal.

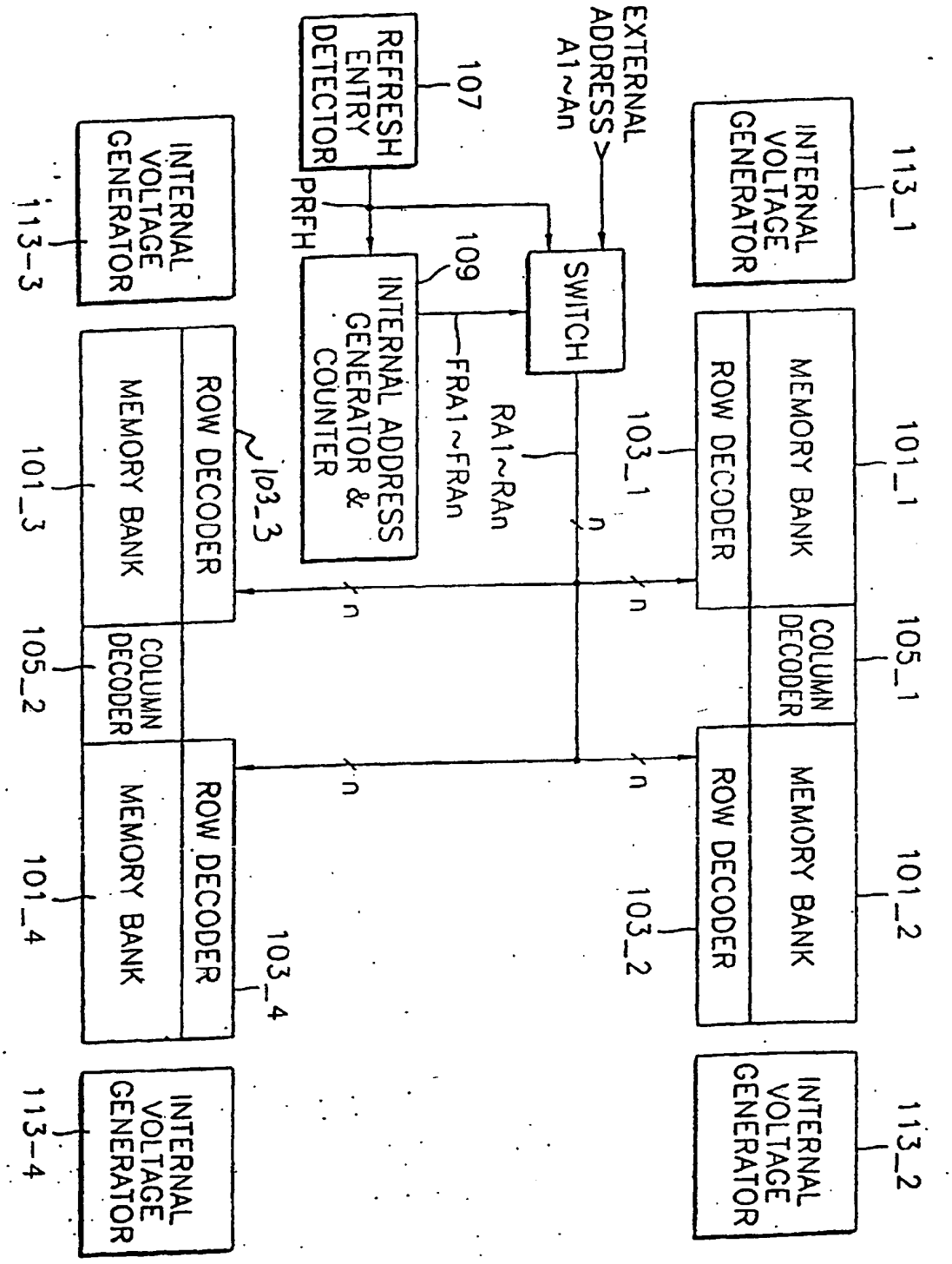
21. A circuit according to Claim 19, further comprising a second pulse generator
wherein the second pulse generator outputs a counter control signal in response to the self-refresh cycle signal to control operation of the counter.

22. A circuit according to Claim 19, further comprising a row address buffer for receiving the row address data output from the counter.

23. A circuit according to Claim 19, further comprising an oscillator for generating an oscillator signal to control operation of the first pulse generator.

24. A circuit according to Claim 23, wherein the first pulse generator comprises a plurality of cycle counters, wherein the oscillator signal is processed by a selected set of cycle counters based on the

FIG. 1 (PRIOR ART)



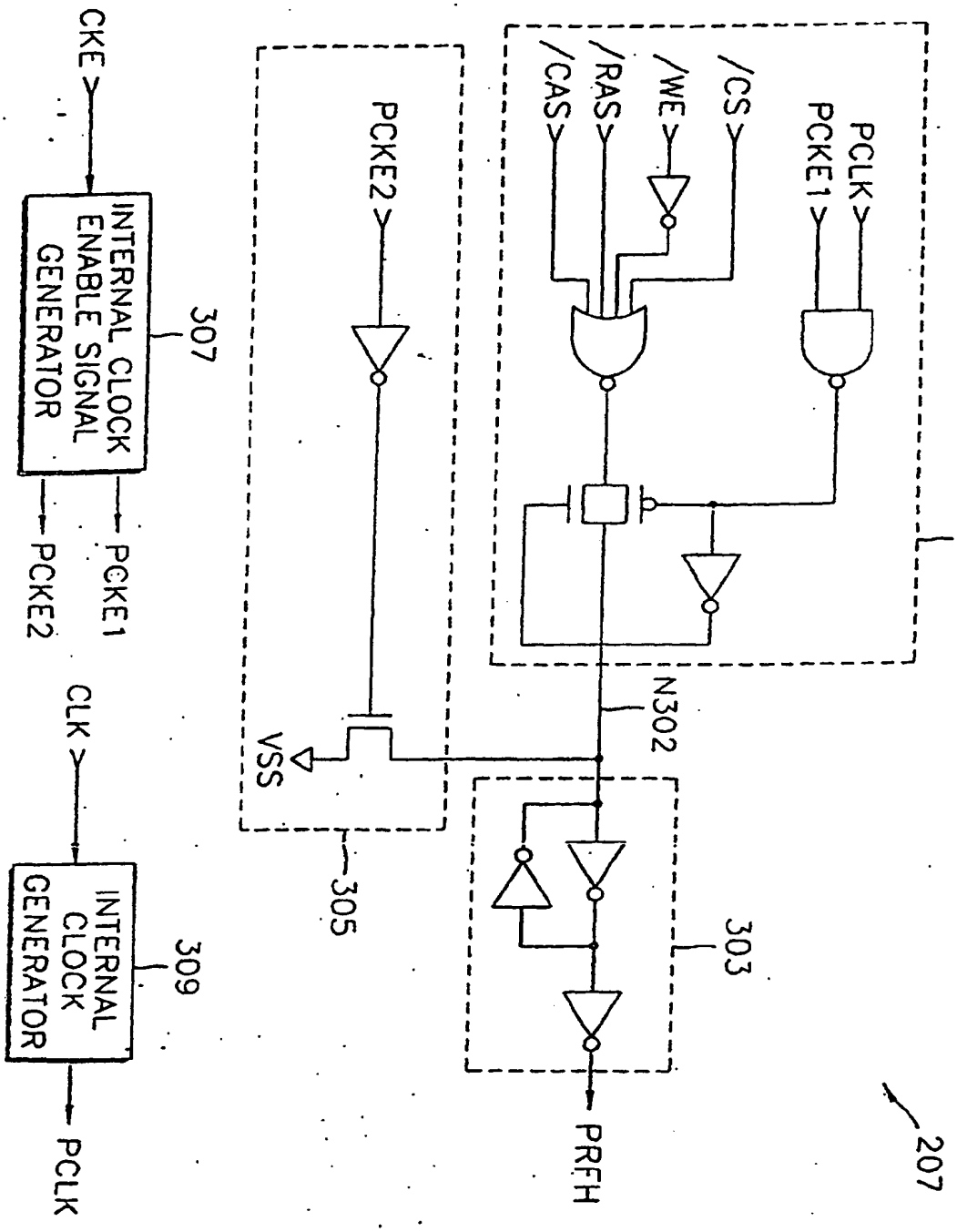

CKE
INTERNAL CLOCK ENABLE SIGNAL GENERATOR
307
PCKE1
PCKE2
CLK
INTERNAL CLOCK GENERATOR
309
PCLK
PCKE2
VSS
305
/CS
/WE
/RAS
/CAS
PCLK
PCKE1
301
N302
303
PRFH
207

FIG. 3

FIG. 5

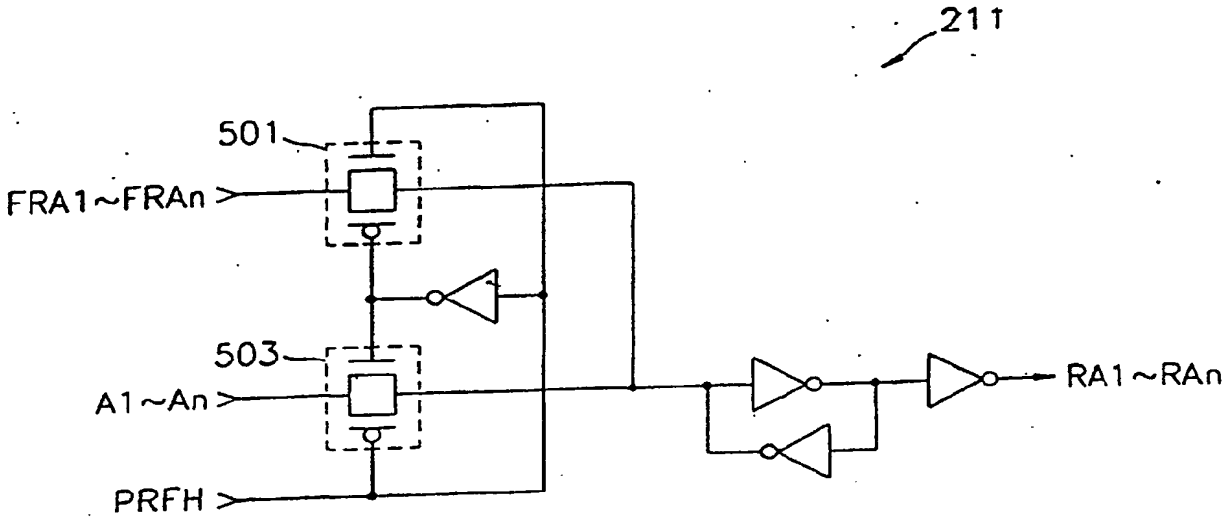

211
501
FRA1~FRAn
503
A1~An
PRFH
RA1~RAn

FIG. 6

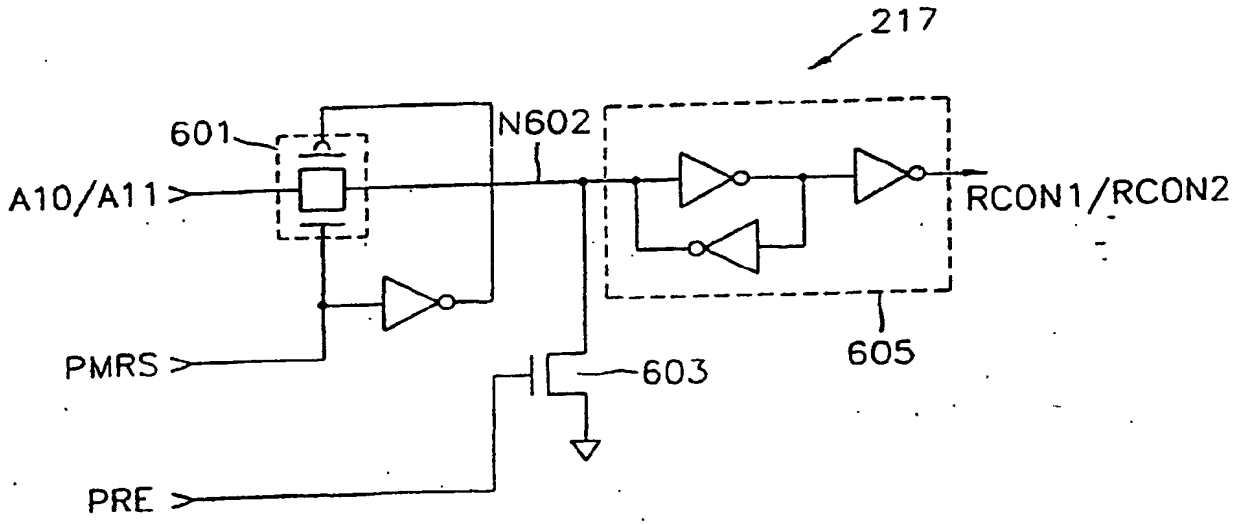

217
601
N602
A10/A11
RCON1/RCON2
PMRS
603
605
PRE

FIG. 9

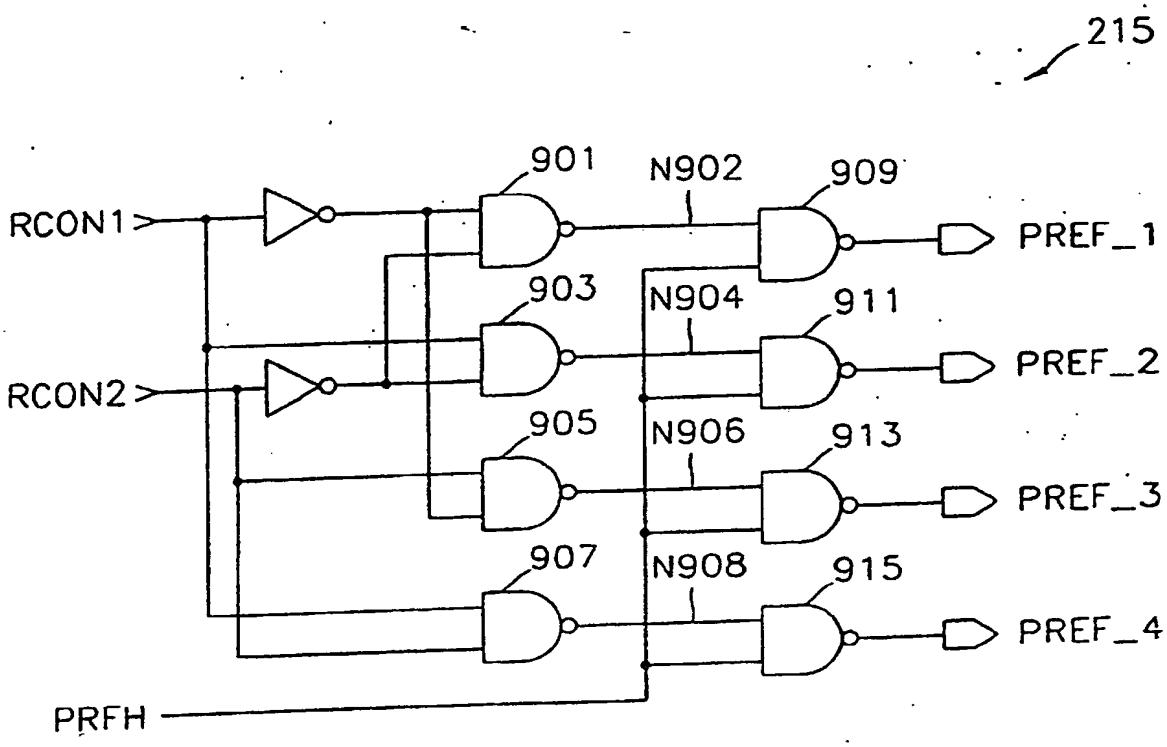

215
901
N902
909
RCON1
PREF_1
903
N904
911
RCON2
PREF_2
905
N906
913
PREF_3
907
N908
915
PREF_4
PRFH

FIG. 11

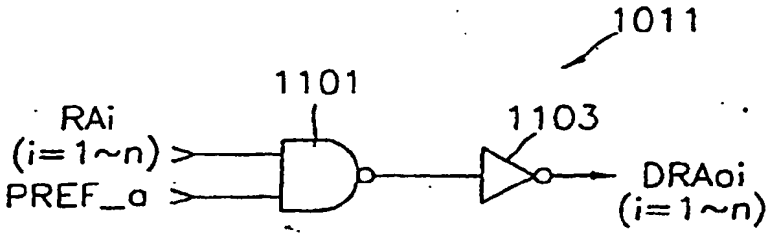

1011
1101
1103
RAi
(i=1~n)
PREF_a
DRAoi
(i=1~n)

FIG. 12

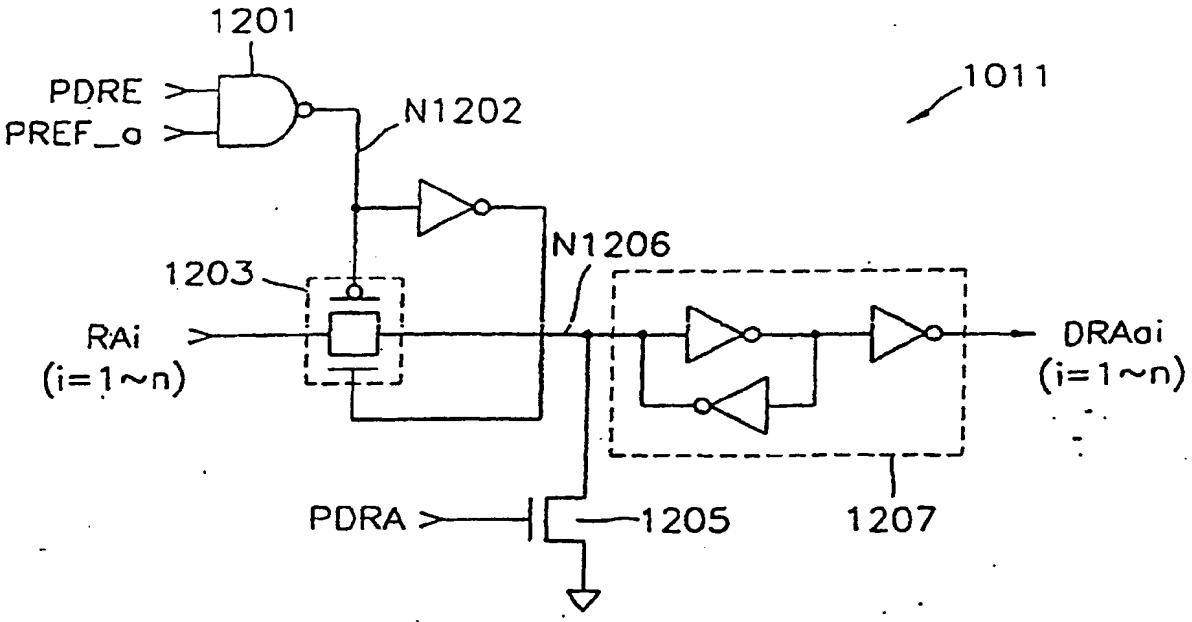
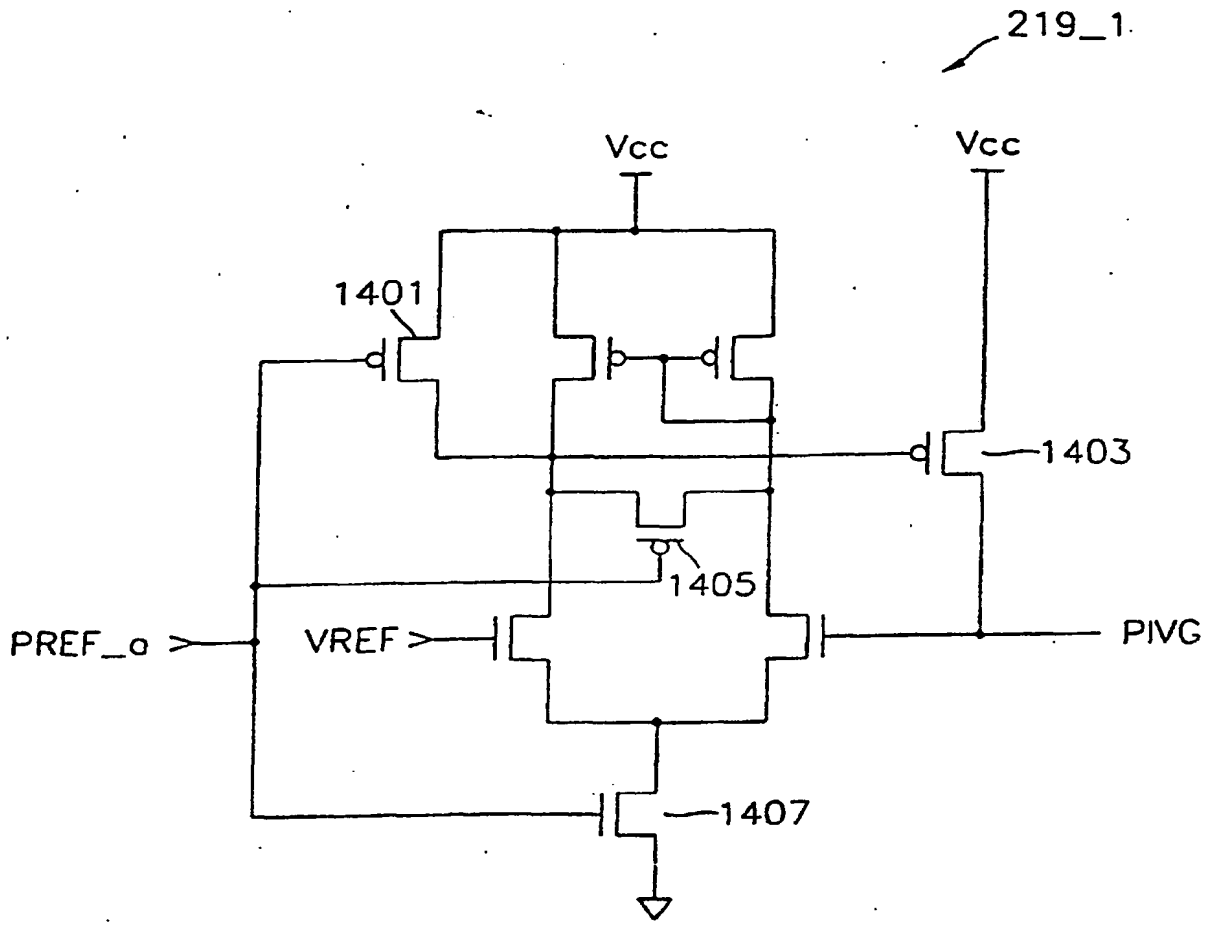

1201
PDRE
PREF_a
N1202
1011
N1206
1203
RAi
(i=1~n)
DRAoi
(i=1~n)
PDRA
1205
1207

FIG. 14



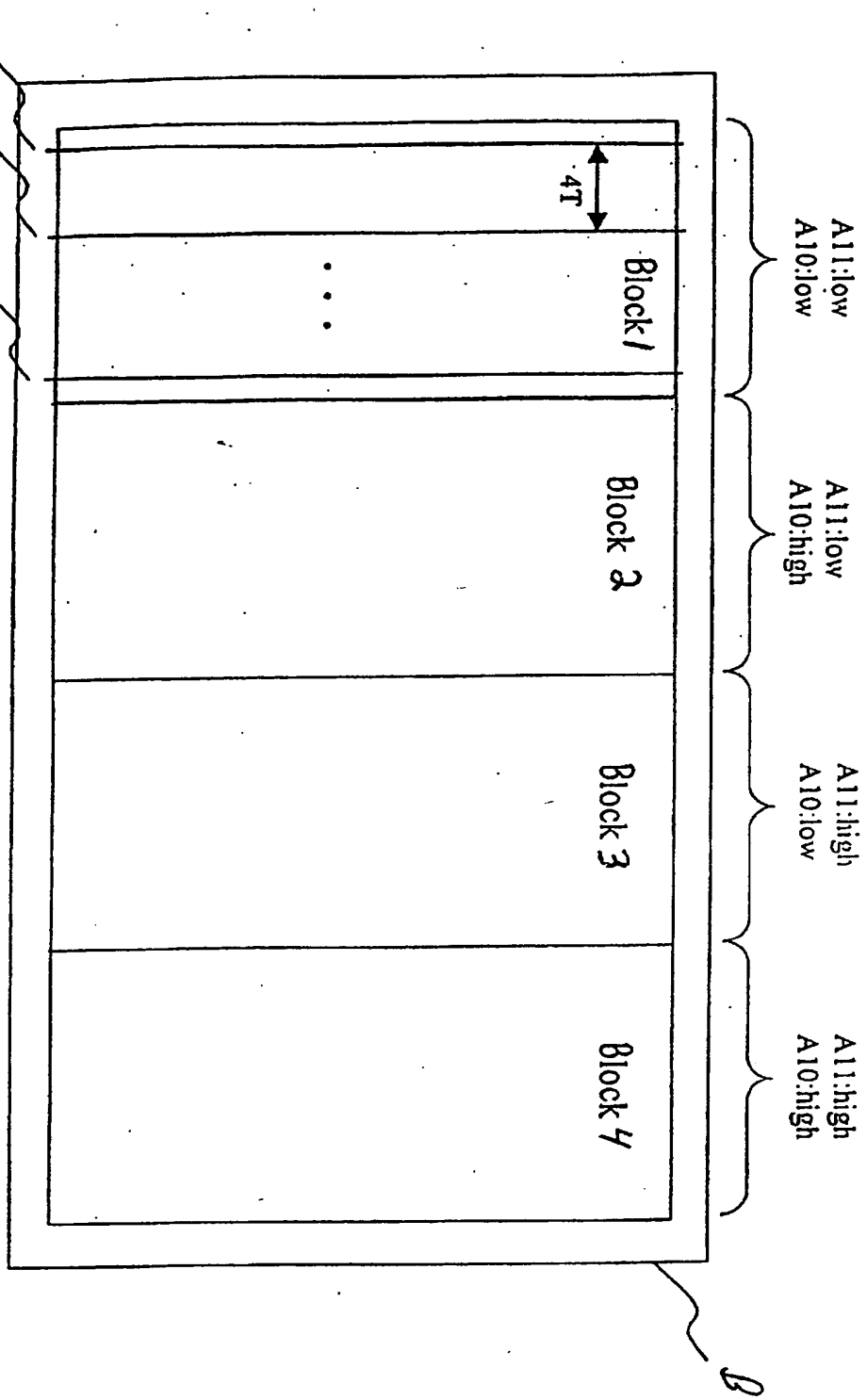

WL0
WL1
WL1023
4T
Block 1
Block 2
Block 3
Block 4
A11:low
A10:low
A11:low
A10:high
A11:high
A10:low
A11:high
A10:high
B

Fig 15(b)

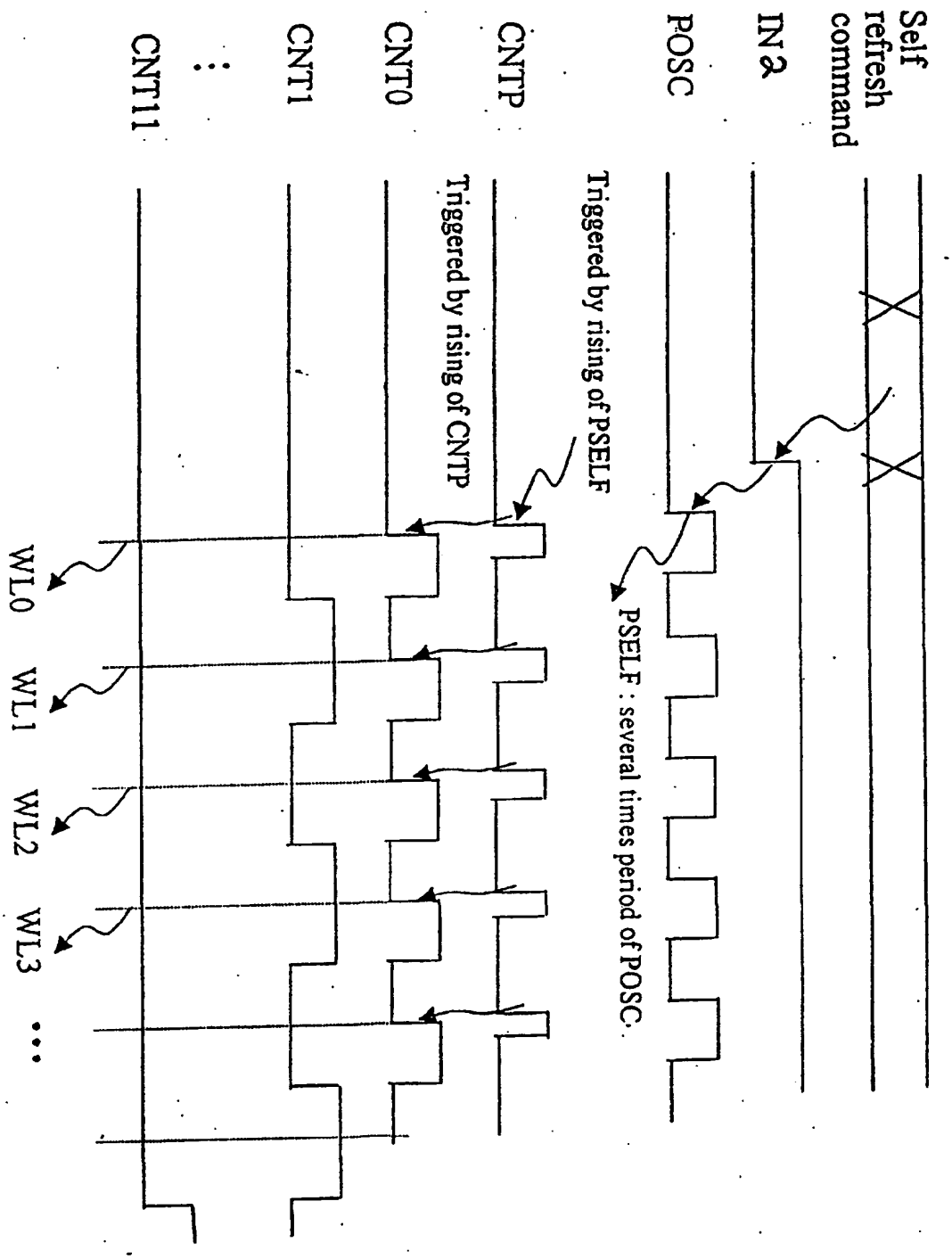

Self refresh command
IN2
POSC
Triggered by rising of PSELF
PSELF : several times period of POSC.
CNTP
Triggered by rising of CNTP
CNT0
CNT1
:
CNT11
WL0
WL1
WL2
WL3
...

Fig. 17

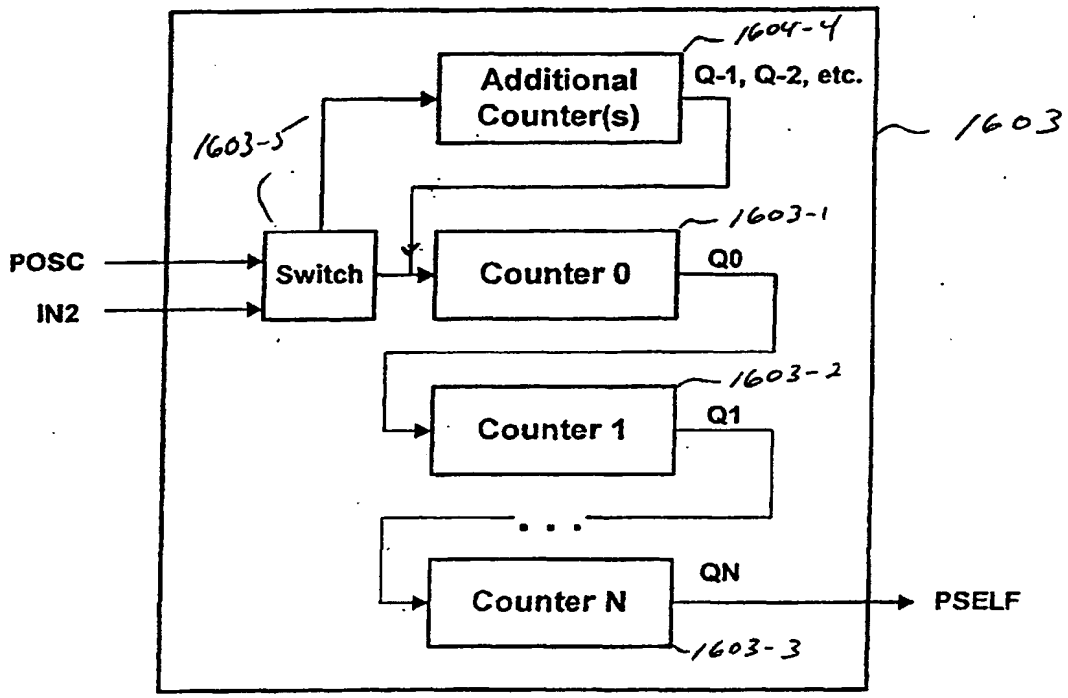

1604-4
Additional Counter(s)
Q-1, Q-2, etc.
1603
1603-5
1603-1
POSC
IN2
Switch
Counter 0
Q0
1603-2
Counter 1
Q1
Counter N
QN
PSELF
1603-3

FIG. 19

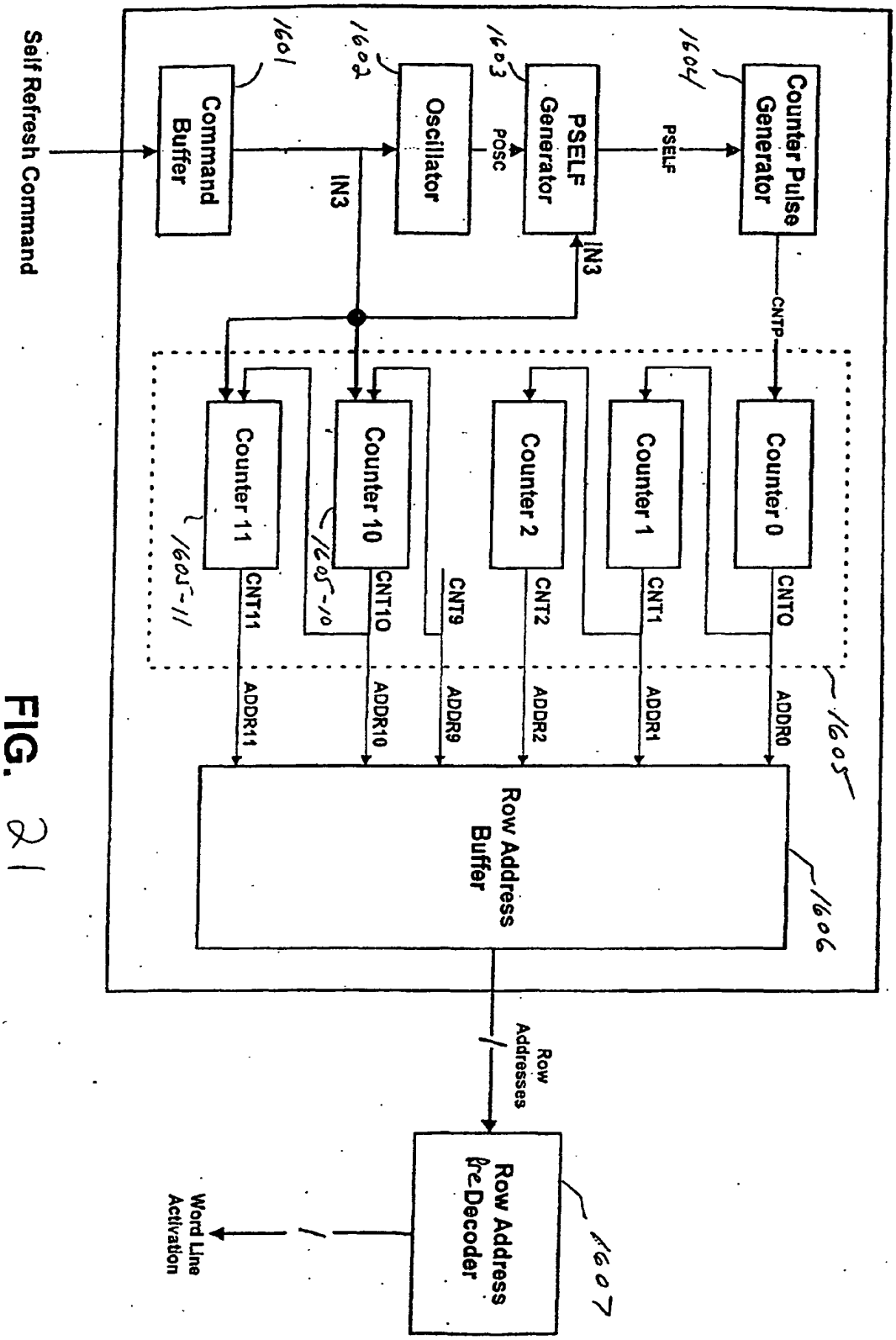

Self Refresh Command
Command Buffer
1601
Oscillator
1602
PSELF Generator
1603
Counter Pulse Generator
1604
IN3
POSC
PSELF
CNTP
Counter 11
Counter 10
Counter 2
Counter 1
Counter 0
1605-11
1605-10
CNT11
CNT10
CNT9
CNT2
CNT1
CNT0
ADDR11
ADDR10
ADDR9
ADDR2
ADDR1
ADDR0
1605
Row Address Buffer
1606
Row Addresses
Row Address Pre-Decoder
1607
Word Line Activation

FIG. 21

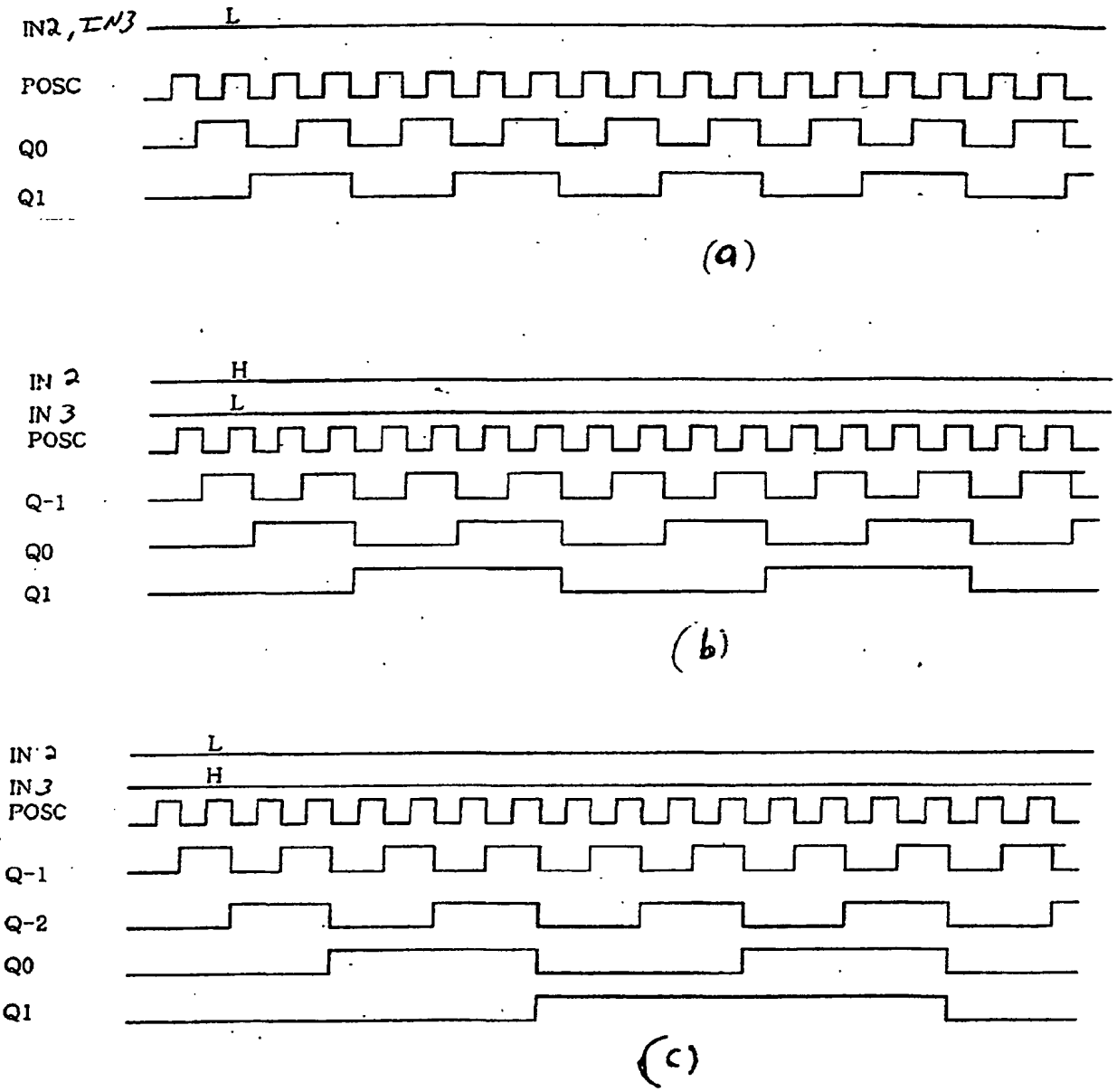

IN2, IN3
L
POSC
Q0
Q1
(a)
IN 2
H
IN 3
L
POSC
Q-1
Q0
Q1
(b)
IN 2
L
IN 3
H
POSC
Q-1
Q-2
Q0
Q1
(c)

Fig 23

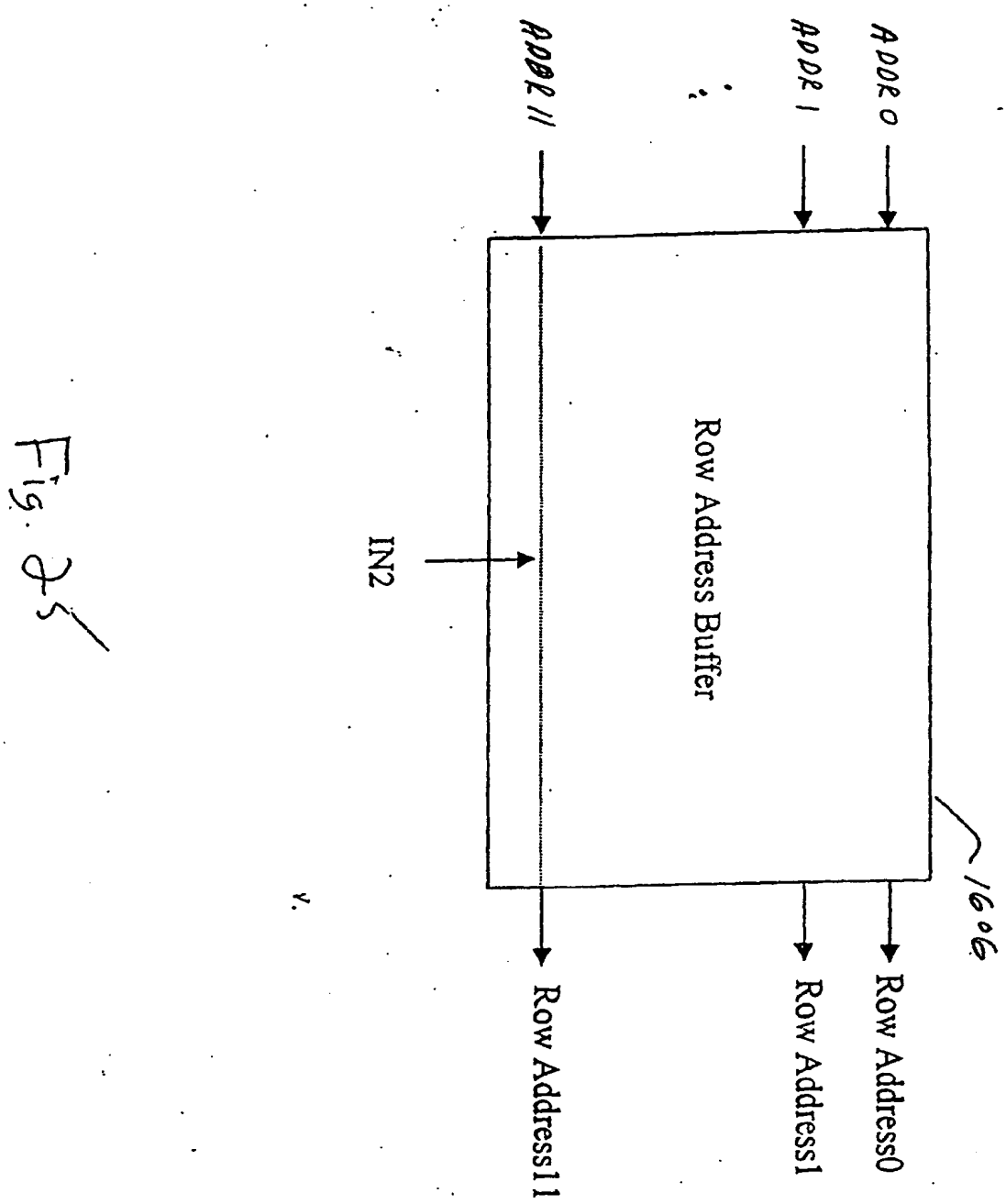

ADDR 0
ADDR 1
ADDR 11
Row Address Buffer
IN2
Row Address0
Row Address1
Row Address11
1606

Fig. 25

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Office européen des brevets

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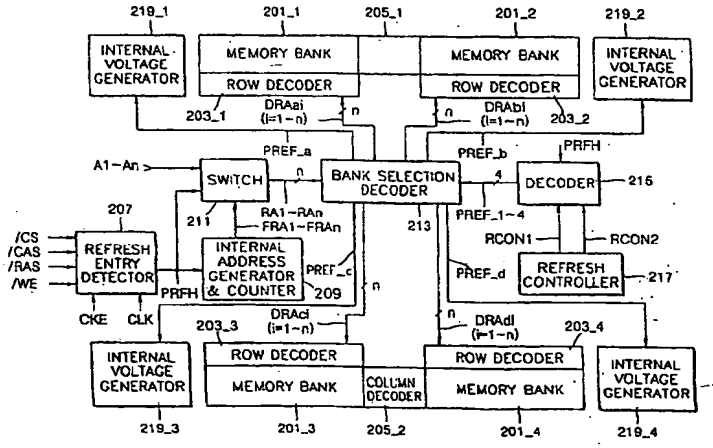
London WC2A 3LS (GB)

(54) System and method for performing partial array self-refresh operation in a semiconductor memory device.

(57) Systems and methods for performing a PASR (partial array self-refresh) operation wherein a refresh operation for recharging stored data is performed on a portion (e.g., ½ 1/4, 1/8, or 1/16) of one or more selected memory banks comprising a cell array in a semiconductor memory device. In one aspect, a PASR operation is performed by (1) controlling the generation of row addresses by a row address counter during a self-refresh operation and (2) controlling a self-refresh cycle generating circuit to adjust the self-refresh cycle output therefrom. The self-refresh cycle is adjusted in a manner that provides a reduction in the current dissipation during the PASR operation. In another aspect, a PASR operation is performed by controlling one or more row addresses corresponding to a partial cell array during a self-refresh operation, whereby a reduction in a self-refresh current dissipation is achieved by blocking the activation of a non-used block of a memory bank.

FIG. 2



EP 1 256 957 A3

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